Signal Name Definitions

The signal names are comprised of:

- An abbreviation of the signal name. An "N" suffix signifies that the signal is active low. Without the "N", the signal is active high.
- The signal's source and destination page numbers.
- An abbreviation of the signal type. There are three types of signals: TTL , V and TRI. TTL stands for digital TTL level, V stands for voltage or an analog signal, and TRI stands for a tri-state digital line such as a data bus.
- A brief description of the signal.

ESI-32 Connectors

Connector CN4 is the floppy DC power header.
Connector CN5 is the option card header.
Connector CN6 is the DC power header.
Connector CN7 is the floppy disk header.
Connector CN8 is the DSP header that was never used.
Connector CN10 is the LCD header.
Connector CN11 is the LCD backlight (HV) power header.
Connector CN13 is the front panel header.

ESI-33, ESI-4000 Connectors

Connector CN2 is the DC power header.
Connector CN3 is the option card header.
Connector CN4 is the floppy DC power header.
Connector CN9 is the floppy disk header.
Connector CN12 is the LCD header.
Connector CN13 is the front panel header.

Signals

Name	Source	Destination	Type	Description
A1	3-B2	4 (CN5), 6, 9, 10, CN1	TTL	CPU Address Bus 1
A2	3-B2	4 (CN5), 6, 9, 10, CN1	TTL	CPU Address Bus 2
A3	3-B2	4 (CN5), 6, 9, 10, CN1	TTL	CPU Address Bus 3
A4	3-B2	4 (CN5), 9, 10, CN1	TTL	CPU Address Bus 4
A5	3-B2	2, 4 (CN5), 9, 10, CN1	TTL	CPU Address Bus 5
A6	3-B2	2, 4 (CN5), 9, 10, CN1	TTL	CPU Address Bus 6
A7	3-B2	2, 4 (CN5), 9, 10, CN1	TTL	CPU Address Bus 7
A8	3-B2	9, 10	TTL	CPU Address Bus 8
A9	3-B2	9, 10	TTL	CPU Address Bus 9
A10	3-B1	9, 10	TTL	CPU Address Bus 10
A11	3-B1	9	TTL	CPU Address Bus 11
A12	3-B1	2, 6, 10	TTL	CPU Address Bus 12
A13	3-B1	5, 10	TTL	CPU Address Bus 13
A14	3-B1	10	TTL	CPU Address Bus 14
A15	3-B1	---	TTL	CPU Address Bus 15
A16	3-B1	---	TTL	CPU Address Bus 16
A17	3-B1	4	TTL	CPU Address Bus 17
A18	3-B1	4	TTL	CPU Address Bus 18
A19	3-B1	4	TTL	CPU Address Bus 19
ADC5VP	8	8	V	Regulated ADC +5V
ADCDATA	8	2	TTL	ADC Data Out
ADCSEL0	3	8	TTL	Input Gain Select 0
ADCSEL1	3	8	TTL	Input Gain Select 1
ADCSEL2	3	8	TTL	Input Gain Select 2
ADCSEL3	3	8, 11	TTL	Input Gain Select 3
ADCSEL4	3	8, 11	TTL	Input Gain Select 4

Name	Source	Destination	Type	Description
AESRXCLK	S/PDIF 1 (CN1)	2, 4 (CN5)	TTL	AES Master Clock
AESRX-DATA	S/PDIF 1 (CN1)	2, 4 (CN5)	TTL	AES Receive Data
BA13	5 (CN10)	LCD	TTL	Buffered Address 13
BD0	5 (CN10) 4 (CN5)	FP 1 (CN7) SCSI 1 (CN1)	TRI TRI	Buffered Data Bus 0(FP) Buffered Data Bus (Expd)
BD1	5 (CN10) 4 (CN5)	FP 1 (CN7) SCSI 1 (CN1)	TRI TRI	Buffered Data Bus 1 (Expd) Buffered Data Bus (Expd)
BD2	5 (CN10) 4 (CN5)	FP 1 (CN7) SCSI 1 (CN1)	TRI TRI	Buffered Data Bus 2 (FP) Buffered Data Bus (Expd)
BD3	5 (CN10) 4 (CN5)	FP 1 (CN7) SCSI 1 (CN1)	TRI TRI	Buffered Data Bus 3 (FP) Buffered Data Bus 3 (Expd)
BD4	5 (CN10) 4 (CN5)	FP 1 (CN7) SCSI 1 (CN1)	TRI TRI	Buffered Data Bus 4 (FP) Buffered Data Bus (Expd)
BD5	5 (CN10) 4 (CN5)	FP 1 (CN7) SCSI 1 (CN1)	TRI TRI	Buffered Data Bus 5 (FP) Buffered Data Bus 5(Expd)
BD6	5 (CN10) 4 (CN5)	FP 1 (CN7) SCSI 1 (CN1)	TRI TRI	Buffered Data Bus 6 (FP) Buffered Data Bus 6(Expd)
BD7	5 (CN10) 4 (CN5)	FP 1 (CN7) SCSI 1 (CN1)	TRI TRI	Buffered Data Bus 7 (FP) Buffered Data Bus 7(Expd)
BSMA0	9 (4000)	9(4000)	TTL	Buffered Snd Mem Addr. 0
BSMA1	9 (4000)	9(4000)	TTL	Buffered Snd Mem Addr. 1
BSMA2	9 (4000)	9(4000)	TTL	Buffered Snd Mem Addr. 2
BSMA3	9 (4000)	9(4000)	TTL	Buffered Snd Mem Addr. 3
BSMA4	9 (4000)	9(4000)	TTL	Buffered Snd Mem Addr. 4
BSMA5	9 (4000)	9(4000)	TTL	Buffered Snd Mem Addr. 5
BSMA6	9 (4000)	9(4000)	TTL	Buffered Snd Mem Addr. 6
BSMA7	9 (4000)	9(4000)	TTL	Buffered Snd Mem Addr. 7
BSMA8	9 (4000)	9(4000)	TTL	Buffered Snd Mem Addr. 8
BSMA9	9 (4000)	9(4000)	TTL	Buffered Snd Mem Addr. 9
BSMA10	9 (4000)	9(4000)	TTL	Buffered Snd Mem Addr. 10
BSMA11	9 (4000)	9(4000)	TTL	Buffered Snd Mem Addr. 11
BSMCAS0	9 (4000)	9(4000)	TTL	Buffered Snd Mem CAS 0
BSMCAS1	9 (4000)	9(4000)	TTL	Buffered Snd Mem CAS 1

Name	Source	Destination	Type	Description
BSMCAS2	9 (4000)	9(4000)	TTL	Buffered Snd Mem CAS 2
BSMCAS3	9 (4000)	9(4000)	TTL	Buffered Snd Mem CAS 3
BSMRAS0	9 (4000)	9(4000)	TTL	Buffered Snd Mem RAS 0
BSMRAS1	9 (4000)	9(4000)	TTL	Buffered Snd Mem RAS 1
BSMRAS2	9 (4000)	9(4000)	TTL	Buffered Snd Mem RAS 2
BSMRAS3	9 (4000)	9(4000)	TTL	Buffered Snd Mem RAS 3
BSMWRN	9 (4000)	9(4000)	TTL	Buffered Snd Mem Write
C3M	6	3	TTL	3 MHz Clock
C16MA	3	4 (CN5), CN1	TTL	16 MHz Clock)
C16MB	3	10 (CN8)	TTL	16 MHz Clock (ESI-32)
C16MB	3	2	TTL	16 MHz Clock (ESI-33, 4000)
C16MC	3	6	TTL	16 MHz Clock
C45M	2	2	TTL	45 MHz Clock
CONTRAST 0	3	5 (CN10), LCD	V	LCD Contrast Voltage
CONTRAST 1	3	5 (CN10), LCD	V	LCD Contrast Voltage
CONTRAST 2	3	5 (CN10), LCD	V	LCD Contrast Voltage
CONTRAST 3	3	5 (CN10), LCD	V	LCD Contrast Voltage
CSBUTRDN	3	5 (CN13), FP 1 (CN7)	TTL	Button Read Chip Select
CSBUT-WRN	3	5 (CN13), FP 1 (CN7)	TTL	Button Write Chip Select
CSDSPN	4	10 (CN8)	TTL	DSP Chip Select
CSDTACKN	3	4	TTL	Data Transfer Ack. CS
CSEXPN	4	2	TTL	Expansion Chip Select
CSFDCN	4	6	TTL	FD Cntlr CS (ESI-32)
CSFDCN	4	2	TTL	FD Cntlr CS (ESI-33, 4000)
CSGCHIPN	4	9	TTL	G-chip Chip Select
CSHCHIPN	4	10	TTL	H-chip Chip Select
CSLCDN	3	6	TTL	LCD Chip Select (ESI-32)

Name	Source	Destination	Type	Description
CSLCDN	3	2	TTL	LCD Chp Sel(ESI-33, 4000)
CSLEDN	3	5 (CN13) FP 1 (CN7)	TTL	LED Chip Select
CSSAM-PLEN	3	6, 8	TTL	ADC Shift Reg CS (ESI-32)
CSSAM-PLEN	2	8	TTL	ADC Shift Reg CS (33, 4000)
D0	3	4, 8, 9, 10	TRI	CPU Data Bus 0
D1	3	4, 8, 9, 10	TRI	CPU Data Bus 1
D2	3	4, 8, 9, 10	TRI	CPU Data Bus 2
D3	3	4, 8, 9, 10	TRI	CPU Data Bus 3
D4	3	4, 8, 9, 10	TRI	CPU Data Bus 4
D5	3	4, 8, 9, 10	TRI	CPU Data Bus 5
D6	3	4, 8, 9, 10	TRI	CPU Data Bus 6
D7	3	4, 8, 9, 10	TRI	CPU Data Bus 7
D8	3	5, 6, 8, 9, 10	TRI	CPU Data Bus 8
D9	3	5, 6, 8, 9, 10	TRI	CPU Data Bus 9
D10	3	5, 6, 8, 9, 10	TRI	CPU Data Bus 10
D11	3	5, 6, 8, 9, 10	TRI	CPU Data Bus 11
D12	3	5, 6, 8, 9, 10	TRI	CPU Data Bus 12
D13	3	5, 6, 8, 9, 10	TRI	CPU Data Bus 13
D14	3	5, 6, 8, 9, 10	TRI	CPU Data Bus 14
D15	3	5, 6, 8, 9, 10	TRI	CPU Data Bus 15
DACCLK	10	4 (CN5), CN1	TTL	DAC Clock
DACDATA	10	4 (CN5), 11, 12, CN1	TTL	DAC Data
DISKRDN	6	6	TTL	Floppy Disk Read Enable
DISKWRN	6	6	TTL	Floppy Disk Write Enable
DSPBOOT	3	10 (CN8)	TTL	Not used(ESI-32)
DSPD-TACKN	10 (CN8)	6	TTL	DSP Data Transfer Ackn.
DTACKN	6, 9, 10	2, 3, 4 (CN5), CN1	TTL	Data Transfer Acknowledge
EEPROMCK	3	4	TTL	EEPROM Clock

Name	Source	Destination	Type	Description
EEPROMCS	3	4	TTL	EEPROM Chip Select
EEPROMDI	3	4	TTL	EEPROM Data In
EEPROMDO	4	3	TTL	EEPROM Data Out
ELCD	6	5 (CN10)	TTL	LCD Enable (ESI-32)
ELCD	2	5 (CN10)	TTL	LCD Enable (ESI-33, 4000)
ENCA	FP 1	5	TTL	Rotary Encoder Data A
ENCB	FP 1	5	TTL	Rotary Encoder Data B
EXPIRQN	SCSI 1 (CN1)	2, 4 (CN5)	TTL	Exp. Int. Req. (Not Used)
FDISKRDN	2	6	TTL	Floppy Disk Read
FDISKWRN	2	6	TTL	Floppy Disk Write
FS1	2	4, 6, 8, CN 1	TTL	Clock x 1 (ESI-32)
FS1	2	2, 4, 8	TTL	Clock x 1 (ESI-33, 4000)
FS2	2	6	TTL	Clock x 2
FS2	2	2	TTL	Clock x 2
FS2N	2	8	TTL	Inverted Clock x 2
FS64	2	4, 8, CN 1	TTL	Clock x 64
FS256A	2	8	TTL	Clock x 256
FS512	2	4, 9 10, CN 1	TTL	Clock x 512
GSRCD	9	10	TTL	SmpRat Cnvrted Data Out
GSYNCN	9	4 (CN5), 10	TTL	G-chip Sync
HA5	10	10	TTL	H-chip Address Bus 5
HA6	10	10	TTL	H-chip Address Bus 6
HA10	10	10	TTL	H-chip Address Bus 10
HDACKN	10	10	TTL	H-chip Address Bus 10
HPAGND	11 (CN2)	FP 1 (CN2)	AGND	Headphone Ground
IRQ1N	2	3	TTL	Interrupt Req. 1 (33, 4000)
JKDET	12	3	VCC	Jack Detect
LSTBN	10	4 (CN5)	TTL	Left DAC Strobe
MAINLCLK	10	11	TTL	DAC Clock, Left
MAINLLEN	10	11	TTL	DAC Latch Enable, Left
MAINRCLK	10	11	TTL	DAC Clock, Right

Name	Source	Destination	Type	Description
MAINRLEN	10	12	TTL	DAC Latch Enable, Right
MIDIRX	7 (CN1)	3	TTL	MIDI Data Receive
MIDITX	3	7	TTL	MIDI Data Transmit
MUTE	12	11	V	Audio Mute
PHONESL	11 (CN2)	FP 1 (CN2)	V	Headphone Out, Left
PHONESR	11 (CN2)	FP 1 (CN2)	V	Headphone Out, Right
RESET	6	2	TTL	System Reset (ESI-32)
RESETN	6	3, 4 (CN5), 8, 9, 10	TTL	Inverted Reset (ESI-32)
RESET	2	2, 6	TTL	System Reset (ESI-33, 4000)
RESETN	2	2, 3, 4, 6, 8, 9, 10	TTL	Inv. Reset (ESI-33, 4000)
RESAMPLE	11	8	V	Audio Self Test (not used)
RETL	12	11	V	Left Submix Return
RETR	12	11	V	Right Submix Return
RSTBN	10	4 (CN5)	TTL	Right DAC Strobe
SCSI	SCSI 1 (CN1)	3, 4 (CN5)	TTL	SCSI Enable
SDISKWRN	2	13 (ESI-33)	TTL	SCSI Enable
SMA0	9	9	TTL	Sound Memory Addr. Bus 0
SMA1	9	9	TTL	Sound Memory Addr. Bus 1
SMA2	9	9	TTL	Sound Memory Addr. Bus 2
SMA3	9	9	TTL	Sound Memory Addr. Bus 3
SMA4	9	9	TTL	Sound Memory Addr. Bus 4
SMA5	9	9	TTL	Sound Memory Addr. Bus 5
SMA6	9	9	TTL	Sound Memory Addr. Bus 6
SMA7	9	9	TTL	Sound Memory Addr. Bus 7
SMA8	9	9	TTL	Sound Memory Addr.Bus 8
SMA9	9	9	TTL	Sound Memory Addr. Bus 9
SMA10	9	9	TTL	Sound Memory Addr. Bus 10
SMA11	9	9	TTL	Sound Memory Addr. Bus 11

Name	Source	Destination	Type	Description
SMCASN	9	9	TTL	Sound RAM CAS
SMD0	9	9	TTL	Sound Memory Data Bus 0
SMD1	9	9	TTL	Sound Memory Data Bus 1
SMD2	9	9	TTL	Sound Memory Data Bus 2
SMD3	9	9	TTL	Sound Memory Data Bus 3
SMD4	9	9	TTL	Sound Memory Data Bus 4
SMD5	9	9	TTL	Sound Memory Data Bus 5
SMD6	9	9	TTL	Sound Memory Data Bus 6
SMD7	9	9	TTL	Sound Memory Data Bus 7
SMD8	9	9	TTL	Sound Memory Data Bus 8
SMD9	9	9	TTL	Sound Memory Data Bus 9
SMD10	9	9	TTL	Sound Memory Data Bus 10
SMD11	9	9	TTL	Sound Memory Data Bus 11
SMD12	9	9	TTL	Sound Memory Data Bus 12
SMD13	9	9	TTL	Sound Memory Data Bus 13
SMD14	9	9	TTL	Sound Memory Data Bus 14
SMD15	9	9	TTL	Sound Memory Data Bus 15
SMDRAM-WRN	9	9 (CN12)	TTL	DRAM Write Enable
SMRASN	9	9	TTL	Sound RAM RAS
SPDIF	S/PDIF 1 (CN1)	3, 4 (CN5)	TTL	S/PDIF Enable
SRDATA	2	8	TTL	Serial Register Data In
SRSEL0	3	2	TTL	Serial Register Select 0
SRSEL1	3	2	TTL	Serial Register Select 1
SUBLCLK	10	12	TTL	DAC Clock, Submix , Left
SUBLLEN	10	12	TTL	DAC Latch Ena. Sub, Left
SUBRCLK	10	12	TTL	DAC Clock, Sub, Right
SUBRLEN	10	12	TTL	DAC Latch Ena. Sub, Right
THRUDIS	3	11	TTL	Audio Feedthru Disable
THRUL	8	11	V	Audio Feedthrough, Left
THRUR	8	11	V	Audio Feedthrough, Right

Name	Source	Destination	Type	Description
VOLUME	FP (CN3)	8 (CN3)	V	Master Volume Control
WRN	3	4 (CN5), 5 (CN10), 6, 9, 10, LCD, CN1	TTL	CPU Write Line

SCSI Option Card

Name	Source	Destination	Type	Description
A1	CN1	1	TTL	CPU Address Bus 1
A2	CN1	1	TTL	CPU Address Bus 2
A3	CN1	1	TTL	CPU Address Bus 3
A4	CN1	1	TTL	CPU Address Bus 4
A5	CN1	1	TTL	CPU Address Bus 5
A6	CN1	1	TTL	CPU Address Bus 6
A7	CN1	1	TTL	CPU Address Bus 7
CSEXPN	CN1	1	TTL	Expansion Chip Select
CSHDCN	1	1	TTL	Hard Disk Cont Chip Select
DISKRDN	1	1	TTL	Disk Read Line
DISKWRN	1	1	TTL	Disk Write Line
DTACKN	CN1	1	TTL	Data Transfer Acknowledge
EXPIRQN	CN1	1	TTL	Expansion Interrupt Request
HDACKN	1	1	TTL	Hard Disk Acknowledge
HDDRQ	1	1	TTL	Hard Disk Data Request
HDIRQ	1	1	TTL	Hard Disk Interrupt Request
HDREQN	1	1	TTL	Hard Disk Request
D0	CN1	1	TRI	CPU Data Bus 0
D1	CN1	1	TRI	CPU Data Bus 1
D2	CN1	1	TRI	CPU Data Bus 2
D3	CN1	1	TRI	CPU Data Bus 3
D4	CN1	1	TRI	CPU Data Bus 4
D5	CN1	1	TRI	CPU Data Bus 5
D6	CN1	1	TRI	CPU Data Bus 6

Name	Source	Destination	Type	Description
D7	CN1	1	TRI	CPU Data Bus 7
RES5380N	1	1	TTL	Reset 5380 Chip
RESETN	CN1	1	TTL	System Reset
SCSI	CN1	1	TTL	SCSI Card Sense Line
UPCLK	CN1	1	TTL	16 MHz Clock
WRN	CN1	1	TTL	CPU Write Line

S/PDIF Option Card

Name	Source	Destination	Type	Description
AES-BOOST	S/PDIF 1	S/PDIF 1	TTL	AES Boost Control
AES-BOOSTN	S/PDIF 1	S/PDIF 1	TTL	Inverted AES Boost
AESINTN	S/PDIF 1	S/PDIF 1	TTL	AES Interrupt
AESPRO	S/PDIF 1	S/PDIF 1	TTL	AES Pro Mode Select
AESPRON	S/PDIF 1	S/PDIF 1	TTL	S/PDIF Select
AESTX-CLK	S/PDIF 1	S/PDIF 1	TTL	AES Transmitter Clock
AESTXLR	S/PDIF 1	S/PDIF 1	TTL	AES Left/Right Sync
AESTXRSTN	S/PDIF 1	S/PDIF 1	TTL	AES Transmitter Reset
CSAES-RXN	S/PDIF 1	S/PDIF 1	TTL	AES Receiver Chip Select
CSEXPN	S/PDIF 1	S/PDIF 1	TTL	Expansion Card Chip Select
ENINT	S/PDIF 1	S/PDIF 1	TTL	Interrupt Enable
EXPIRQN	S/PDIF 1	S/PDIF 1	TTL	Exp. Card Interrupt Request
HSTB0N	S/PDIF 1	S/PDIF 1	TTL	H-chip Strobe 0
HSTB1N	S/PDIF 1	S/PDIF 1	TTL	H-chip Strobe 1

Turbo Option Card

Name	Source	Destination	Type	Description
A1	1 (CN1)	1, 2	TTL	CPU Address Bus 1
A2	1 (CN1)	1, 2	TTL	CPU Address Bus 2
A3	1 (CN1)	1, 2	TTL	CPU Address Bus 3
A4	1 (CN1)	1, 2	TTL	CPU Address Bus 4
A5	1 (CN1)	1, 2	TTL	CPU Address Bus 5
A6	1 (CN1)	2	TTL	CPU Address Bus 6
A7	1 (CN1)	2	TTL	CPU Address Bus 7
AESRX-CLK	1 (CN1)	1	TTL	AES Master Clock
AESRX-DATA	1 (CN1)	1	TTL	AES Receiver Data
CSAES-RXN	2	1	TTL	AES Receiver Chip Select
CSG05N	2	2	TTL	G.05 Chip Select
CSEXPN	1 (CN1)	2	TTL	Expansion Chip Select
DACCLK	2	3, 4, 5	TTL	DAC Clock
DACDATA	2	3, 4, 5	TTL	DAC Data
DTACKN	2	1 (CN1)	TTL	Data Transfer Acknowledge
D0	1 (CN1)	1, 2	TRI	CPU Data Bus 0
D1	1 (CN1)	1, 2	TRI	CPU Data Bus 1
D2	1 (CN1)	1, 2	TRI	CPU Data Bus 2
D3	1 (CN1)	1, 2	TRI	CPU Data Bus 3
D4	1 (CN1)	1, 2	TRI	CPU Data Bus 4
D5	1 (CN1)	1, 2	TRI	CPU Data Bus 5
D6	1 (CN1)	1, 2	TRI	CPU Data Bus 6
D7	1 (CN1)	1, 2	TRI	CPU Data Bus 7
FS1	1 (CN1)	1	TTL	Clock x 1
FS64	1 (CN1)	1	TTL	Clock x 64
FS512	1 (CN1)	1, 2	TTL	Clock x 512
FS512BUF	1	2	TTL	Buffered Clock x 512
FXOUTLL	2	3	TTL	FX Out L-Chan Latch Enab
FXOUTLR	2	3	TTL	FX Out R-Chan Latch Enab

Name	Source	Destination	Type	Description
G05OSC	1	2	TTL	G.05 Clock
G05RDN	2	2	TTL	G.05 Read Line
G05RSTN	2	2	TTL	G.05 Reset Line
G05WAITN	2	2	TTL	G.05 Wait Line
G05WRN	2	2	TTL	G.05 Write Line
HCLK	1 (CN1)	2	TTL	DAC Clock
HDATA	1 (CN1)	2	TTL	DAC Data
HSRB7	1	2	TTL	H-Chip Strobe 7
JDETA	4	2	TTL	Jack Detect A
JDETB	5	2	TTL	Jack Detect B
MSTB7	1 (CN1)	2	TTL	DAC Latch Enable
MUTE	4	3, 4, 5	V	Output Mute Control
RESETN	1 (CN1)	2	TTL	Inverted Reset
SAABC	2	2	TTL	Synchr. Aux Audio Bit Clock
SAAD	2	2	TTL	Synchron. Aux. Audio Data
SAAWC	2	2	TTL	Sync Aux Audio Word Clock
SPDIFOUT	2	1	TTL	G.05 S/PDIF Out
SUB2LL	2	4	TTL	Sub 2 L-Chan Latch Enable
SUB2LR	2	4	TTL	Sub 2 R-Chan Latch Enable
SUB3LL	2	5	TTL	Sub 3 L-Chan Latch Enable
SUB3LR	2	5	TTL	Sub 3 R-Chan Latch Enable
UPCLK	1 (CN1)	2	TTL	16 MHz Clock
WRN	1 (CN1)	1, 2	TTL	CPU Write Line

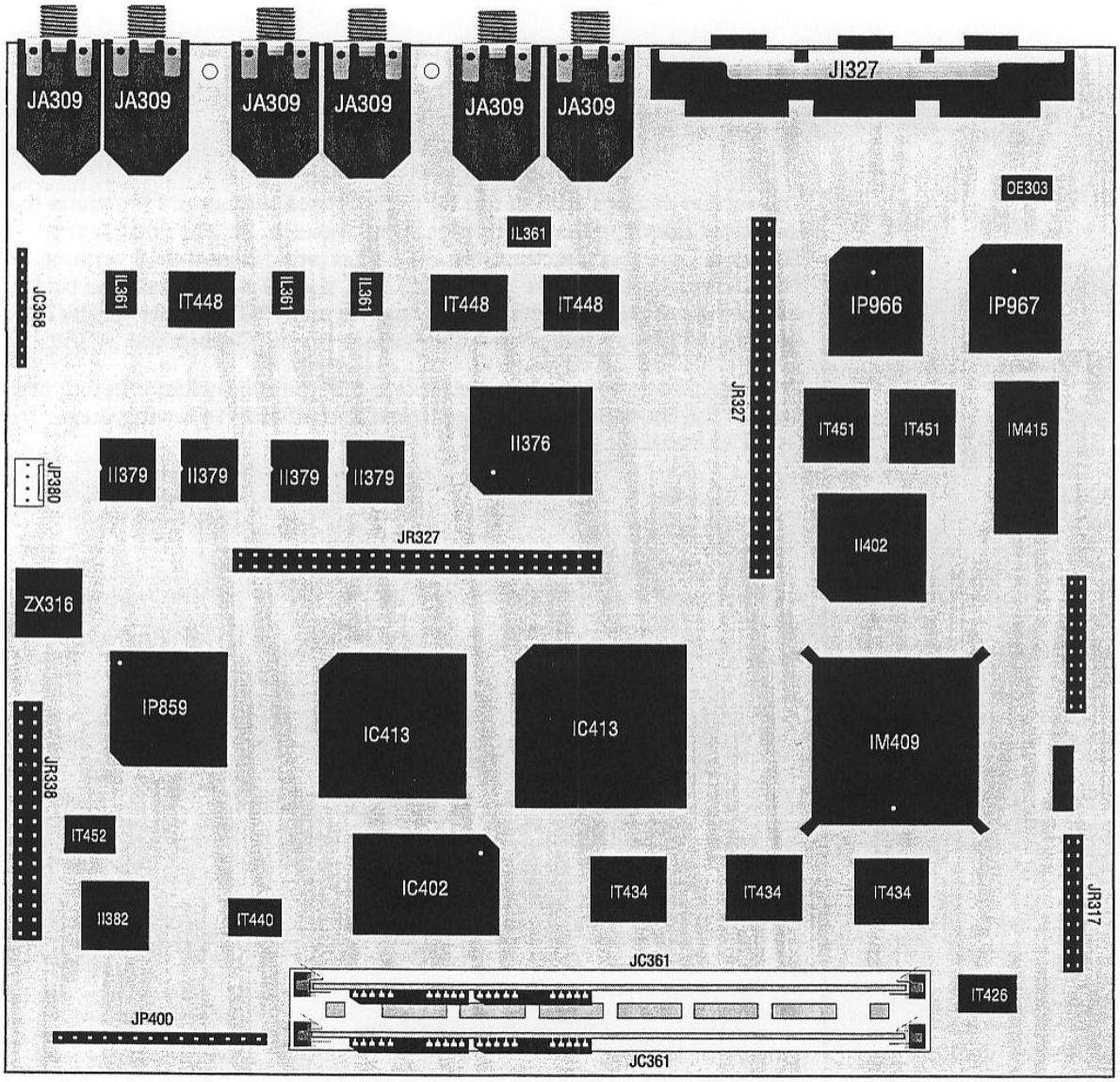
ESI Parts

This section displays each of the ESI circuit board layouts and illustrates the integrated circuit and connector locations for each. As described in the Theory of Operations section, the ESI-32 has two different PCB versions. This section starts with the newest ESI PCB, the ESI 4000, then goes back chronologically to the oldest. Following the main PCB layouts are the ESI option card layouts and pinout illustrations for the G-Chip and H-Chip.

Use these illustrations to help you locate part numbers when ordering new parts. A full list of ESI parts can be found immediately following these layout illustrations.

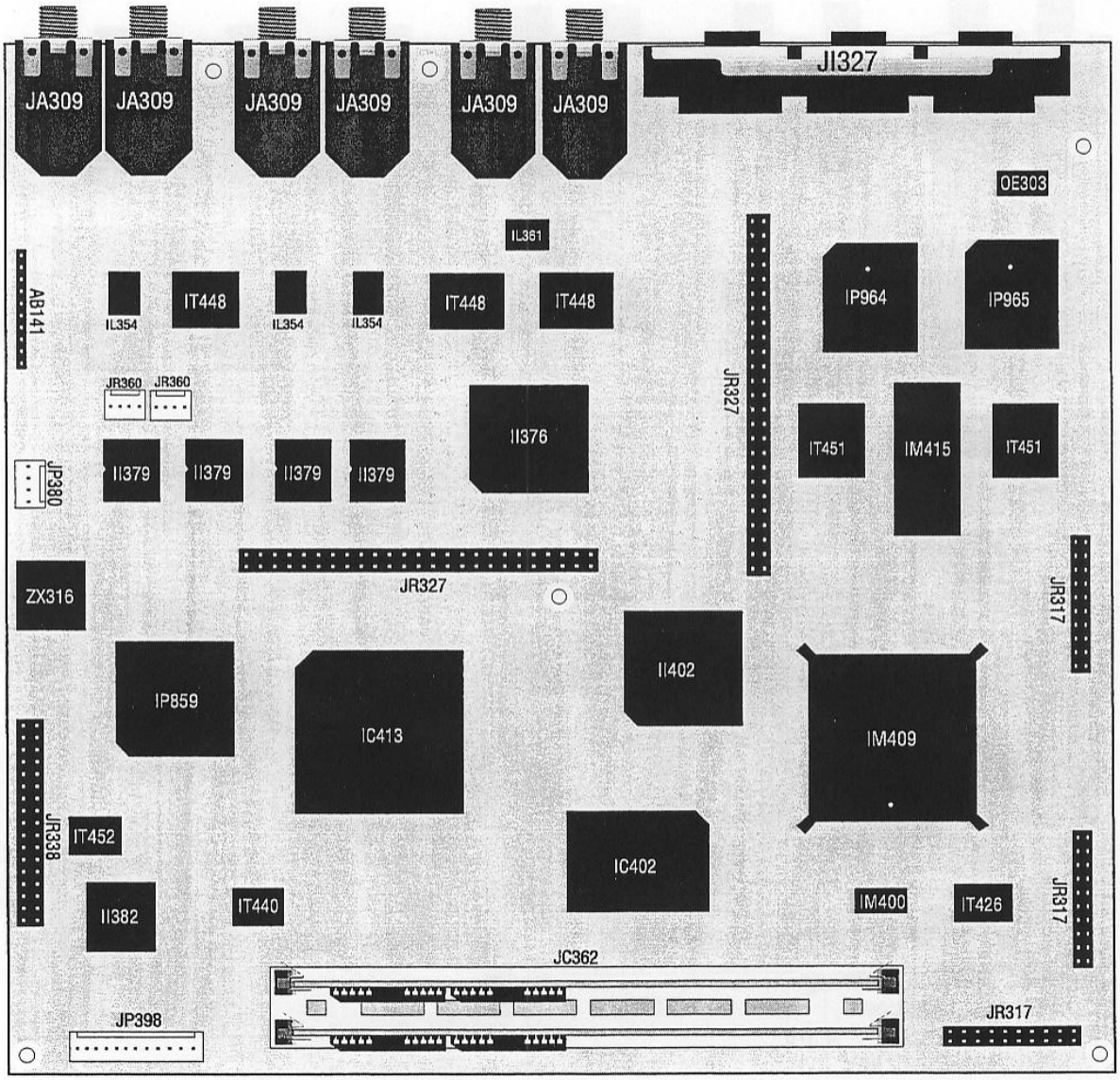
ESI 4000 Main PCB Layout

The following illustration displays the IC and Connector locations on the ESI 4000 main printed circuit board.



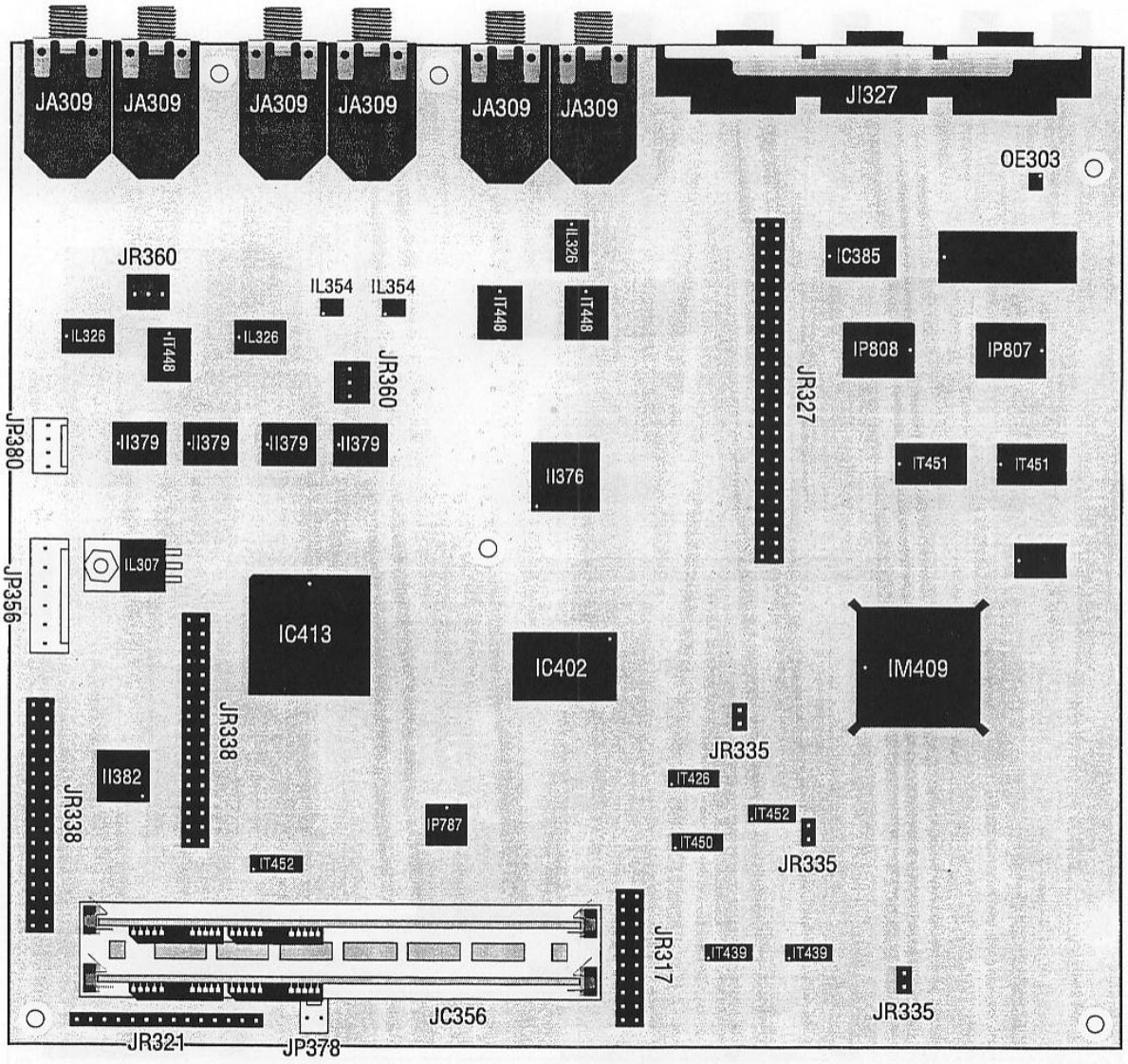
ESI-33 Main PCB Layout

The following illustration displays the IC and Connector locations on the latest version ESI-33 main printed circuit board.



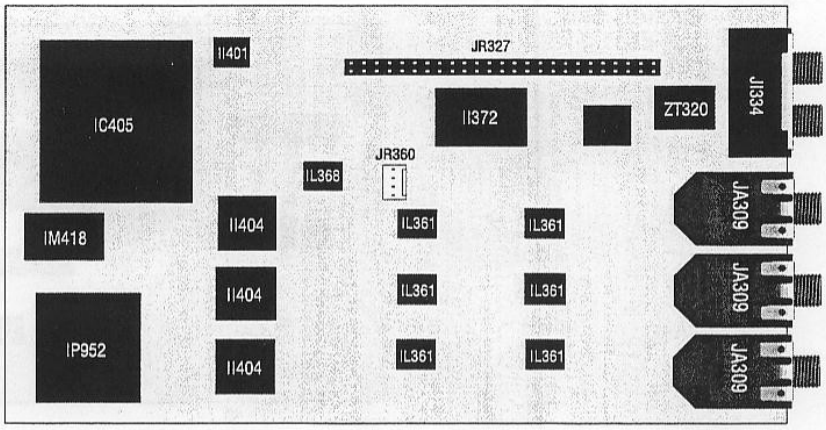
ESI-32 Main PCB Layout

The following illustration displays the IC and Connector locations on the earliest version ESI-32 main printed circuit board.



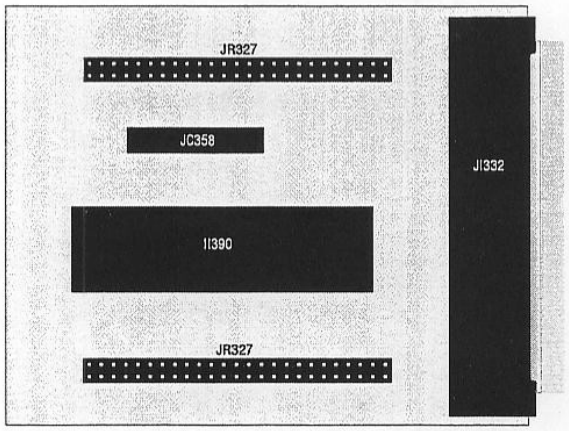
ESI Turbo Option PCB Layout

The following illustration displays the IC and Connector locations on the ESI Turbo Option printed circuit board.



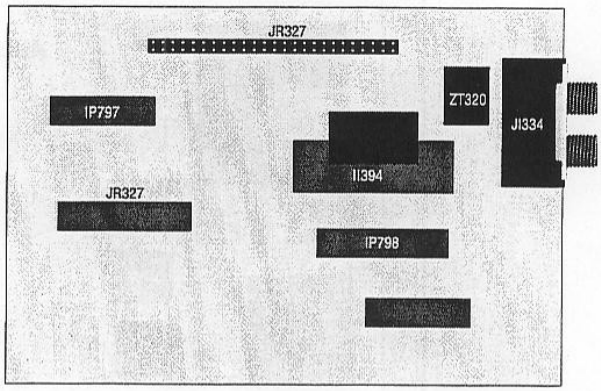
ESI SCSI Option PCB Layout

The following illustration displays the IC and Connector locations on the ESI SCSI Option printed circuit board.

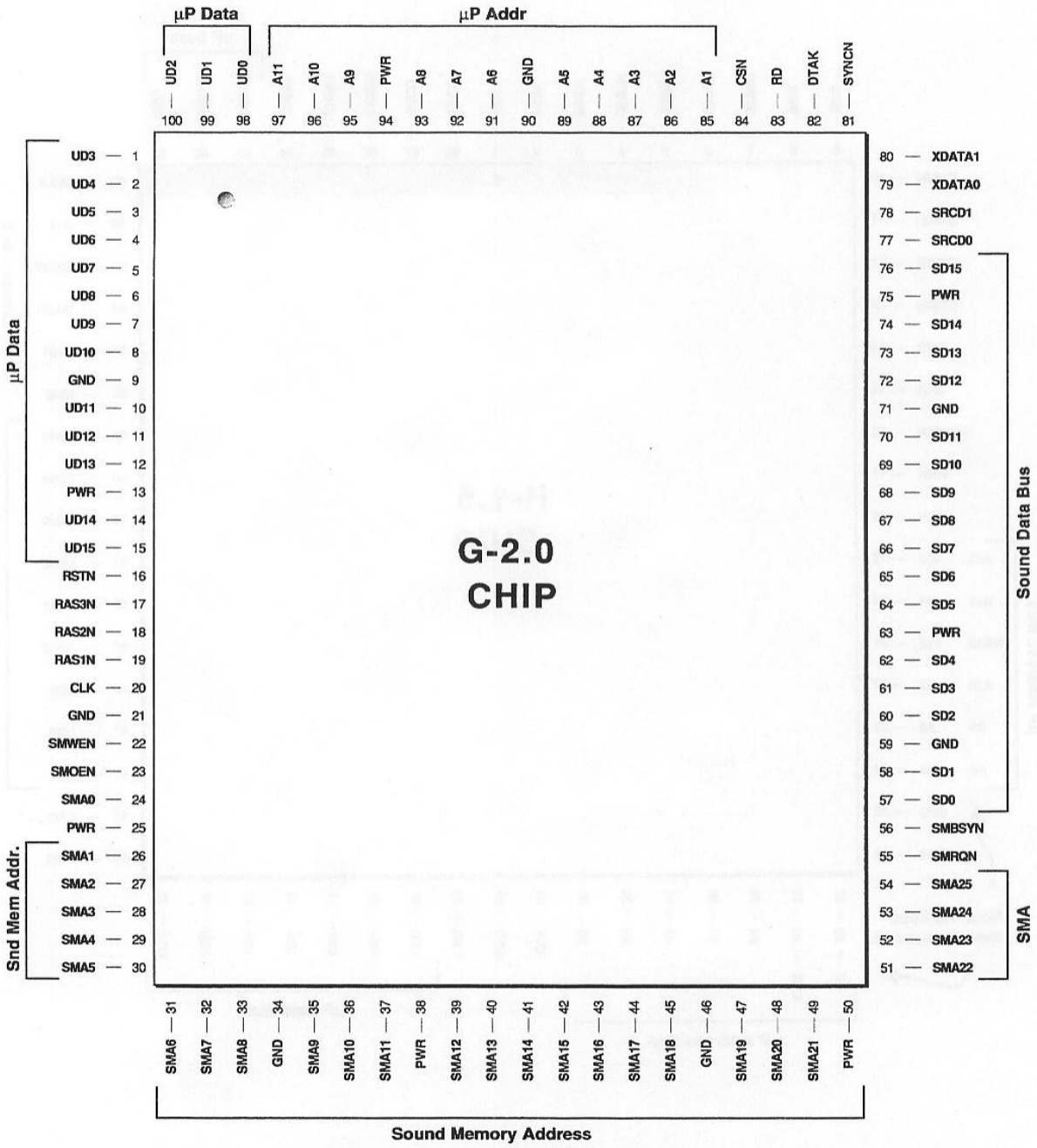


ESI S/PDIF Option PCB Layout

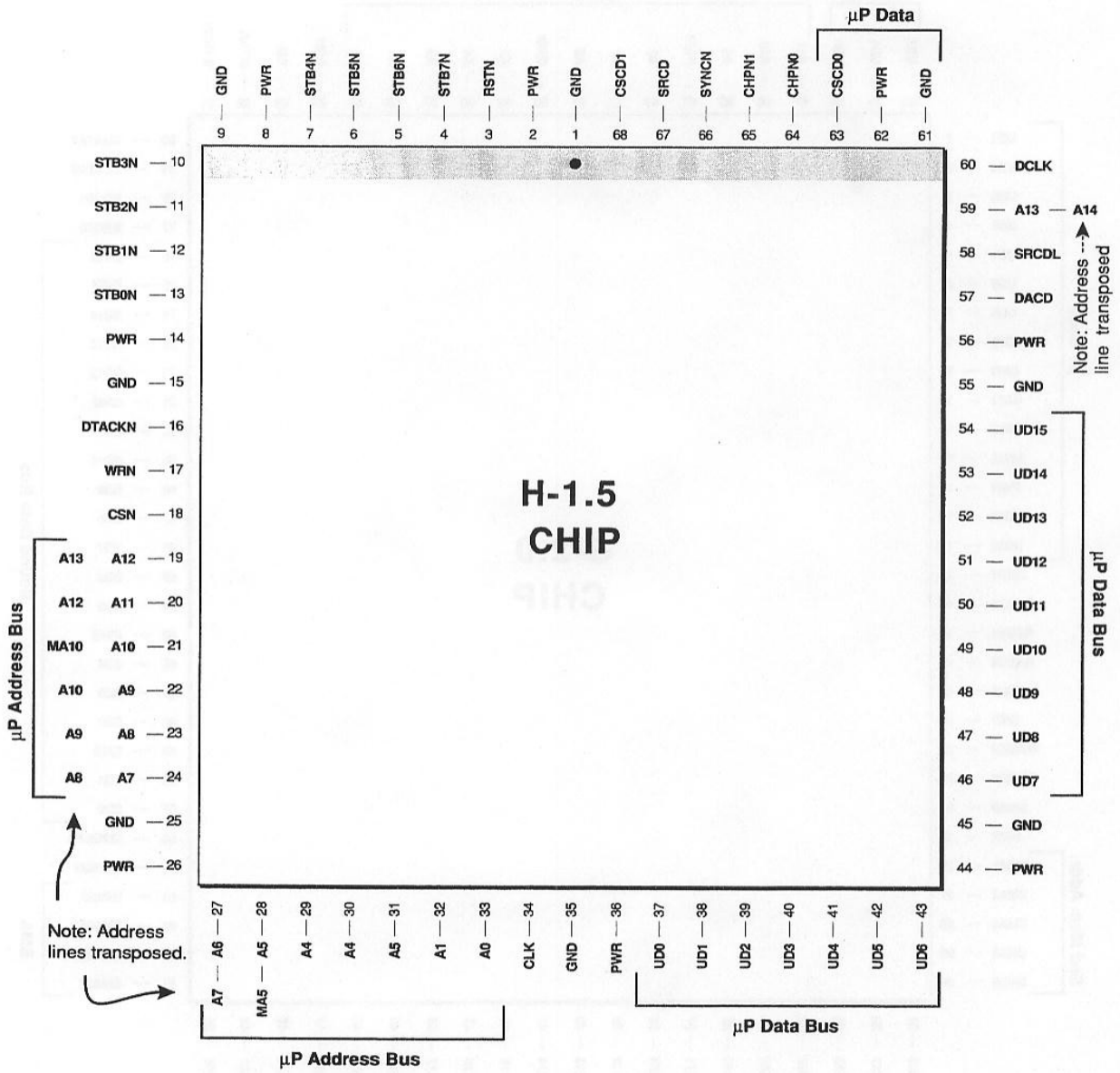
The following illustration displays the IC and Connector locations on the ESI S/PDIF Option printed circuit board.



G-Chip Pinout



H-Chip Pinout



Assembly Drawings